nRF52810

Engineering A

Errata

v1.0

Contents

Chapter 1
nRF52810 Engineering A Errata

This Errata document contains anomalies for the nRF52810 chip, revision Engineering A (QFAA-BB0, QCAA-CB0, CAAA-AA0).

Chapter 2
Change log

See the following list for an overview of changes from previous versions of this document.

Version	Date	Change
nRF52810 Engineering A v1.0	12.07.2017	• Added: No. 15. "RAM[x].POWERSET/CLR read as zero" • Added: No. 20. "Register values are invalid" • Added: No. 31. "Calibration values are not correctly loaded from FICR at reset" • Added: No. 36. "Some registers are not reset when expected" • Added: No. 66. "Linearity specification not met with default settings" • Added: No. 68. "EVENTS_HFCLKSTARTED can be generated before HFCLK is stable" • Added: No. 77. "RC oscillator is not calibrated when first started" • Added: No. 78. "High current consumption when using timer STOP task only" • Added: No. 81. "PIN_CNF is not retained when in debug interface mode" • Added: No. 83. "STOPPED event occurs twice if the STOP task is triggered during a transaction" • Added: No. 88. "Increased current consumption when configured to pause in System ON idle" • Added: No. 103. "Reset value of CCM.MAXPACKETSIZE causes encryption, decryption, and MIC failures" • Added: No. 136. "Bits in RESETREAS are set when they should not be" • Added: No. 150. "EVENT_STARTED does not fire" • Added: No. 155. "IN event may occur more than once on input edge" • Added: No. 156. "Some CLR tasks give unintentional behavior"

Chapter 3
New and inherited anomalies

The following anomalies are present in revision Engineering A of the nRF52810 chip.

Table 1: New and inherited anomalies

ID	Module	Description	New in Engineering A
15	POWER	RAM[x].POWERSET/CLR read as zero	X
20	RTC	Register values are invalid	X
31	CLOCK	Calibration values are not correctly loaded from FICR at reset	X
36	CLOCK	Some registers are not reset when expected	X
66	TEMP	Linearity specification not met with default settings	X
68	CLOCK	EVENTS_HFCLKSTARTED can be generated before HFCLK is stable	X
77	CLOCK	RC oscillator is not calibrated when first started	X
78	TIMER	High current consumption when using timer STOP task only	X
81	GPIO	PIN_CNF is not retained when in debug interface mode	X
83	TWIS	STOPPED event occurs twice if the STOP task is triggered during a transaction	X
88	WDT	Increased current consumption when configured to pause in System ON idle	X
103	CCM	Reset value of CCM.MAXPACKETSIZE causes encryption, decryption, and MIC failures	X
136	System	Bits in RESETREAS are set when they should not be	X
150	SAADC	EVENT_STARTED does not fire	X
155	GPIOTE	IN event may occur more than once on input edge	X
156	GPIOTE	Some CLR tasks give unintentional behavior	X

3.1 [15] POWER: RAM[x].POWERSET/CLR read as zero

This anomaly applies to IC Rev. Engineering A, build codes QFAA-BB0, QCAA-CB0, CAAA-AA0.

Symptoms

RAM[x].POWERSET and RAM[x].POWERCLR read as zero, even though the RAM is on.

Conditions

Always.

Consequences

Not possible to read the RAM state using RAM[x].POWERSET and RAM[x].POWERCLR registers. Write works as it should.

Workaround

Use RAM[x].POWER to read the state of the RAM.

3.2 [20] RTC: Register values are invalid

This anomaly applies to IC Rev. Engineering A, build codes QFAA-BB0, QCAA-CB0, CAAA-AA0.

Symptoms

RTC registers will not contain the correct/expected value if read.

Conditions

The RTC has been idle.

Consequences

RTC configuration cannot be determined by reading RTC registers.

Workaround

Execute the below code before you use RTC.

```
NRF_CLOCK->EVENTS_LFCLKSTARTED  = 0;
NRF_CLOCK->TASKS_LFCLKSTART     = 1;
while (NRF_CLOCK->EVENTS_LFCLKSTARTED == 0) {}
NRF_RTC0->TASKS_STOP = 0;
```

3.3 [31] CLOCK: Calibration values are not correctly loaded from FICR at reset

This anomaly applies to IC Rev. Engineering A, build codes QFAA-BB0, QCAA-CB0, CAAA-AA0.

Symptoms

RCOSC32KICALLENGTH is initialized with the wrong FICR value.

Conditions

Always

Consequences

RCOSC32KICALLENGTH default value is wrong.

Workaround

Execute the following code after reset:

```
*(volatile uint32_t *)0x4000053C = ((*(volatile uint32_t *)0x10000244) &
0x0000E000) >> 13;
```

```
```

This code is already present in the latest system_nrf52.c file.

3.4 [36] CLOCK: Some registers are not reset when expected

This anomaly applies to IC Rev. Engineering A, build codes QFAA-BB0, QCAA-CB0, CAAA-AA0.

Symptoms

After watchdog timeout reset, CPU lockup reset, soft reset, or pin reset, the following CLOCK peripheral registers are not reset:

- CLOCK->EVENTS_DONE
- CLOCK->EVENTS_CTTO
- CLOCK->CTIV

Conditions

After watchdog timeout reset, CPU Lockup reset, soft reset, and pin reset.

Consequences

Register reset values might be incorrect. It may cause undesired interrupts in case of enabling interrupts without clearing the DONE or CTTO events.

Workaround

Clear affected registers after reset. This workaround has already been added into system_nrf52.c file. This workaround has already been added into system_nrf52840.c file present in MDK 8.11.0 or later.

3.5 [66] TEMP: Linearity specification not met with default settings

This anomaly applies to IC Rev. Engineering A, build codes QFAA-BB0, QCAA-CB0, CAAA-AA0.

Symptoms

TEMP module provides non-linear temperature readings over the specified temperature range.

Conditions

Always

Consequences

TEMP module returns out of spec temperature readings.

Workaround

Execute the following code after reset:

```
        NRF_TEMP->A0 = NRF_FICR->TEMP.A0;
        NRF_TEMP->A1 = NRF_FICR->TEMP.A1;
        NRF_TEMP->A2 = NRF_FICR->TEMP.A2;
        NRF_TEMP->A3 = NRF_FICR->TEMP.A3;
        NRF_TEMP->A4 = NRF_FICR->TEMP.A4;
```

```
        NRF_TEMP->A5 = NRF_FICR->TEMP.A5;
        NRF_TEMP->B0 = NRF_FICR->TEMP.B0;
        NRF_TEMP->B1 = NRF_FICR->TEMP.B1;
        NRF_TEMP->B2 = NRF_FICR->TEMP.B2;
        NRF_TEMP->B3 = NRF_FICR->TEMP.B3;
        NRF_TEMP->B4 = NRF_FICR->TEMP.B4;
        NRF_TEMP->B5 = NRF_FICR->TEMP.B5;
        NRF_TEMP->T0 = NRF_FICR->TEMP.T0;
        NRF_TEMP->T1 = NRF_FICR->TEMP.T1;
        NRF_TEMP->T2 = NRF_FICR->TEMP.T2;
        NRF_TEMP->T3 = NRF_FICR->TEMP.T3;
        NRF_TEMP->T4 = NRF_FICR->TEMP.T4;
```

This code is already present in the latest system_nrf52.c file and in the system_nrf52840.c file released in MDK 8.12.0.

3.6 [68] CLOCK: EVENTS_HFCLKSTARTED can be generated before HFCLK is stable

This anomaly applies to IC Rev. Engineering A, build codes QFAA-BB0, QCAA-CB0, CAAA-AA0.

Symptoms

EVENTS_HFCLKSTARTED may come before HFXO is started.

Conditions

When using a 32 MHz crystal with start-up longer than 400 µs.

Consequences

Performance of radio and peripheral requiring HFXO will be degraded until the crystal is stable.

Workaround

32 MHz crystal oscillator startup time must be verified by the user. If the worst-case startup time is shorter than 400 µs, no workaround is required. If the startup time can be longer than 400 µs, the software must ensure, using a timer, that the crystal has had enough time to start up before using peripherals that require the HFXO. The Radio requires the HFXO to be stable before use. The ADC, TIMERs, and TEMP sensor for example can use the HFXO as a reference for improved accuracy.

3.7 [77] CLOCK: RC oscillator is not calibrated when first started

This anomaly applies to IC Rev. Engineering A, build codes QFAA-BB0, QCAA-CB0, CAAA-AA0.

Symptoms

The LFCLK RC oscillator frequency can have a frequency error of up to -25 to +40% after reset. A +/- 2% error is stated in the Product Specification.

Conditions

Always

Consequences

The LFCLK RC oscillator frequency is inaccurate.

Workaround

Calibrate the LFCLK RC oscillator before its first use after a reset.

3.8 [78] TIMER: High current consumption when using timer STOP task only

This anomaly applies to IC Rev. Engineering A, build codes QFAA-BB0, QCAA-CB0, CAAA-AA0.

Symptoms

Increased current consumption when the timer has been running and the STOP task is used to stop it.

Conditions

The timer has been running (after triggering a START task) and then it is stopped using a STOP task only.

Consequences

Increased current consumption

Workaround

Use the SHUTDOWN task after the STOP task or instead of the STOP task.

3.9 [81] GPIO: PIN_CNF is not retained when in debug interface mode

This anomaly applies to IC Rev. Engineering A, build codes QFAA-BB0, QCAA-CB0, CAAA-AA0.

Symptoms

GPIO pin configuration is reset on wakeup from System OFF.

Conditions

The system is in debug interface mode.

Consequences

GPIO state unreliable until PIN_CNF is reconfigured.

3.10 [83] TWIS: STOPPED event occurs twice if the STOP task is triggered during a transaction

This anomaly applies to IC Rev. Engineering A, build codes QFAA-BB0, QCAA-CB0, CAAA-AA0.

Symptoms

STOPPED event is set after clearing it.

Conditions

The STOP task is triggered during a transaction.

Consequences

STOPPED event occurs twice: When the STOP task is fired and when the master issues a stop condition on the bus. This could provoke an extra interrupt or a failure in the TWIS driver.

Workaround

The last STOPPED event must be accounted for in software.

3.11 [88] WDT: Increased current consumption when configured to pause in System ON idle

This anomaly applies to IC Rev. Engineering A, build codes QFAA-BB0, QCAA-CB0, CAAA-AA0.

Symptoms

Using the mode where watchdog is paused in CPU Idle, the current consumption jumps from 3 µA to 400 µA.

Conditions

When we enable WDT with the CONFIG option to pause when CPU sleeps:

```
NRF_WDT->CONFIG = (WDT_CONFIG_SLEEP_Pause<<WDT_CONFIG_SLEEP_Pos);
```

Consequences

Reduced battery life

Workaround

Do not enter System ON IDLE within 125 µs after reloading the watchdog.

3.12 [103] CCM: Reset value of CCM.MAXPACKETSIZE causes encryption, decryption, and MIC failures

This anomaly applies to IC Rev. Engineering A, build codes QFAA-BB0, QCAA-CB0, CAAA-AA0.

Symptoms

Failing encryption, decryption, and MIC on extended length packets.

Conditions

Always for extended length packets.

Consequences

Failing encryption, decryption, and MIC on extended length packets.

Workaround

Set CCM.MAXPACKETSIZE to 0xFB.

This workaround has already been added into the system_nrf52840.c file present in MDK 8.11.1 or later.

3.13 [136] System: Bits in RESETREAS are set when they should not be

This anomaly applies to IC Rev. Engineering A, build codes QFAA-BB0, QCAA-CB0, CAAA-AA0.

Symptoms

After pin reset, RESETREAS bits other than RESETPIN might also be set.

Conditions

A pin reset has triggered.

Consequences

If the firmware evaluates RESETREAS, it might take the wrong action.

Workaround

When RESETREAS shows a pin reset (RESETPIN), ignore other reset reason bits.

Important: RESETREAS bits must be cleared between resets.

Apply the following code after any reset:

```
if (NRF_POWER->RESETREAS & POWER_RESETREAS_RESETPIN_Msk){
    NRF_POWER->RESETREAS =  ~POWER_RESETREAS_RESETPIN_Msk;
}
```

This workaround is implemented in MDK version 8.13.0 and later.

3.14 [150] SAADC: EVENT_STARTED does not fire

This anomaly applies to IC Rev. Engineering A, build codes QFAA-BB0, QCAA-CB0, CAAA-AA0.

Symptoms

EVENT_STARTED does not fire.

Conditions

ADC started (TASKS_START) with PPI task. Any channel configured to TACQ <= 5 µs.

Consequences

ADC cannot be started (TASKS_START) with PPI if TACQ <= 5 µs.

Workaround

Use TAQC > 5 µs when starting ADC from PPI.

3.15 [155] GPIOTE: IN event may occur more than once on input edge

This anomaly applies to IC Rev. Engineering A, build codes QFAA-BB0, QCAA-CB0, CAAA-AA0.

Symptoms

IN event occurs more than once on an input edge.

Conditions

Input signal edges are closer together than 1.3 µs or >= 750 kHz for a periodic signal.

Consequences

Tasks connected through PPI or SHORTS to this event might be triggered twice.

Workaround

Apply the following code when any GPIOTE channel is configured to generate an IN event on edges that can occur within 1.3 µs of each other:

```
*(volatile uint32_t *)(NRF_GPIOTE_BASE + 0x600 + (4 * GPIOTE_CH_USED)) =
 1;
```

Important: A clock is kept on by the workaround and must be reverted to avoid higher current consumption when GPIOTE is not in use, using the following code:

```
*(volatile uint32_t *)(NRF_GPIOTE_BASE + 0x600 + (4 *
 GPIOTE_CH_USED)) = 0;
```

3.16 [156] GPIOTE: Some CLR tasks give unintentional behavior

This anomaly applies to IC Rev. Engineering A, build codes QFAA-BB0, QCAA-CB0, CAAA-AA0.

Symptoms

One of the following:

- Current consumption is high when entering IDLE.
- Latency for detection changes on inputs connected to GPIOTE channels becoming longer that expected.

Conditions

Using the following tasks:

Address	GPIOTE task
0x060	TASK_CLR[0]
0x064	TASK_CLR[1]
0x068	TASK_CLR[2]
0x06C	TASK_CLR[3]
0x070	TASK_CLR[4]
0x074	TASK_CLR[5]
0x078	TASK_CLR[6]
0x07C	TASK_CLR[7]

Consequences

High current consumption or too long time from external event to internal triggering of PPI event and/or IRQ from GPIOTE.

Using TASK_CLR[*n*] for even values of *n* has the side effect of setting the system in constant latency mode (see POWER->TASKS_CONSTLAT). Using TASK_CLR[*n*] for odd values of *n* has the side effect of setting the system in low power mode (see POWER->TASKS_LOWPOWER).

Workaround

To set the system back in the mode it was before using the TASK_CLR[*n*], triggering of tasks with even *n* must be followed by triggering any of the TASK_CLR with odd *n* and vice versa.

All rights reserved.
Reproduction in whole or in part is prohibited without the prior written permission of the copyright holder.