nRF52840 Engineering A Errata

v1.0

Contents

Chapter 1
nRF52840 Engineering A Errata

This Errata document contains anomalies for the nRF52840 chip, revision Engineering A (QIAA-AA0).

Chapter 2
Change log

See the following list for an overview of changes from previous versions of this document.

Table 1: Change log

Version	Date	Change
nRF52840 Engineering A v1.0	06.12.2016	• Added: No. 15. "RAM[x].POWERSET/CLR read as zero" • Added: No. 20. "Register values are invalid" • Added: No. 36. "Some registers are not reset when expected" • Added: No. 51. "Aligned stereo slave mode does not work" • Added: No. 54. "Wrong LRCK polarity in Aligned mode" • Added: No. 55. "RXPTRUPD and TXPTRUPD events asserted after STOP" • Added: No. 58. "An additional byte is clocked out when RXD.MAXCNT = 1" • Added: No. 66. "Linearity specification not met with default settings" • Added: No. 68. "EVENTS_HFCLKSTARTED can be generated before HFCLK is stable" • Added: No. 81. "PIN_CNF is not retained when in debug interface mode" • Added: No. 83. "STOPPED event occurs twice if the STOP task is triggered during a transaction" • Added: No. 87. "Unexpected wake from System ON Idle when using FPU" • Added: No. 89. "Static 400 µA current while using GPIOTE" • Added: No. 94. "BUSSTATE register is not functional" • Added: No. 96. "DMA buffers can only be located in the first 64 kB of data RAM" • Added: No. 98. "Not able to communicate with the peer" • Added: No. 101. "Sleep current increases after soft reset" • Added: No. 103. "Reset value of CCM.MAXPACKETSIZE causes encryption, decryption, and MIC failures" • Added: No. 104. "EPDATA event is not always generated" • Added: No. 110. "Packet loss or degraded sensitivity" • Added: No. 111. "Retention in OFF mode is not controlled by RAM[n].POWER->SxRETENTION, but by RAM[n].POWER->SxPOWER " • Added: No. 112. "False SFD field matches in IEEE 802.15.4 mode RX" • Added: No. 113. "Single-ended mode with external reference is not functional" • Added: No. 115. "RAM content cannot be trusted upon waking up from System ON Idle or System OFF mode" • Added: No. 116. "HFCLK not stopped when entering into SENSE_FIELD state" • Added: No. 117. "Reading address 0x40029618 blocks the device" • Added: No. 118. "Reading halfwords or bytes from the XIP region is not supported" • Added: No. 119. "Wake up from System OFF on V_{BUS} detect is not functional"

Version	Date	Change
		• Added: No. 121. “Second read and long read commands fail” • Added: No. 122. “QSPI uses current after being disabled” • Added: No. 127. “Two stop bit setting is not functional” • Added: No. 128. “RATIO register is not functional” • Added: No. 129. “Reading EPSTALL register causes undefined behavior” • Added: No. 130. “Writing to certain read-only registers causes undefined behavior” • Added: No. 131. “EasyDMA transfer size is limited to 255 bytes” • Added: No. 133. “NRF_RADIO->EVENTS_BCMATCH event might trigger twice” • Added: No. 134. “ISOINCONFIG register is not functional” • Added: No. 135. “SIZE.ISOOUT register does not report empty incoming packets” • Added: No. 136. “Bits in RESETREAS are set when they should not be” • Added: No. 140. “REG0 External circuitry supply in LDO mode is not functional in System ON IDLE ” • Added: No. 142. “Sensitivity not according to specification”

Chapter 3
New and inherited anomalies

The following anomalies are present in revision Engineering A of the nRF52840 chip.

Table 2: New and inherited anomalies

ID	Module	Description	New in Engineering A
15	POWER	RAM[x].POWERSET/CLR read as zero	X
20	RTC	Register values are invalid	X
36	CLOCK	Some registers are not reset when expected	X
51	I2S	Aligned stereo slave mode does not work	X
54	I2S	Wrong LRCK polarity in Aligned mode	X
55	I2S	RXPTRUPD and TXPTRUPD events asserted after STOP	X
58	SPIM	An additional byte is clocked out when RXD.MAXCNT = 1	X
66	TEMP	Linearity specification not met with default settings	X
68	CLOCK	EVENTS_HFCLKSTARTED can be generated before HFCLK is stable	X
81	GPIO	PIN_CNF is not retained when in debug interface mode	X
83	TWIS	STOPPED event occurs twice if the STOP task is triggered during a transaction	X
87	CPU	Unexpected wake from System ON Idle when using FPU	X
89	TWI	Static 400 µA current while using GPIOTE	X
94	USBD	BUSSTATE register is not functional	X
96	I2S	DMA buffers can only be located in the first 64 kB of data RAM	X
98	NFCT	Not able to communicate with the peer	X
101	CLOCK	Sleep current increases after soft reset	X
103	CCM	Reset value of CCM.MAXPACKETSIZE causes encryption, decryption, and MIC failures	X
104	USBD	EPDATA event is not always generated	X
110	RADIO	Packet loss or degraded sensitivity	X
111	RAM	Retention in OFF mode is not controlled by RAM[n].POWER->SxRETENTION, but by RAM[n].POWER->SxPOWER	X
112	RADIO	False SFD field matches in IEEE 802.15.4 mode RX	X
113	COMP	Single-ended mode with external reference is not functional	X
115	RAM	RAM content cannot be trusted upon waking up from System ON Idle or System OFF mode	X

ID	Module	Description	New in Engineering A
116	NFCT	HFCLK not stopped when entering into SENSE_FIELD state	X
117	System	Reading address 0x40029618 blocks the device	X
118	QSPI	Reading halfwords or bytes from the XIP region is not supported	X
119	POWER	Wake up from System OFF on V_{BUS} detect is not functional	X
121	QSPI	Second read and long read commands fail	X
122	QSPI	QSPI uses current after being disabled	X
127	UARTE	Two stop bit setting is not functional	X
128	PDM	RATIO register is not functional	X
129	USBD	Reading EPSTALL register causes undefined behavior	X
130	USBD	Writing to certain read-only registers causes undefined behavior	X
131	UARTE	EasyDMA transfer size is limited to 255 bytes	X
133	CLOCK,RADIO	NRF_RADIO->EVENTS_BCMATCH event might trigger twice	X
134	USBD	ISOINCONFIG register is not functional	X
135	USBD	SIZE.ISOOUT register does not report empty incoming packets	X
136	System	Bits in RESETREAS are set when they should not be	X
140	POWER	REG0 External circuitry supply in LDO mode is not functional in System ON IDLE	X
142	RADIO	Sensitivity not according to specification	X

3.1 [15] POWER: RAM[x].POWERSET/CLR read as zero

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

RAM[x].POWERSET and RAM[x].POWERCLR read as zero, even though the RAM is on.

Conditions

Always.

Consequences

Not possible to read the RAM state using RAM[x].POWERSET and RAM[x].POWERCLR registers. Write works as it should.

Workaround

Use RAM[x].POWER to read the state of the RAM.

3.2 [20] RTC: Register values are invalid

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

RTC registers will not contain the correct/expected value if read.

Conditions

The RTC has been idle.

Consequences

RTC configuration cannot be determined by reading RTC registers.

Workaround

Execute the below code before you use RTC.

```
NRF_CLOCK->EVENTS_LFCLKSTARTED  = 0;
NRF_CLOCK->TASKS_LFCLKSTART     = 1;
while (NRF_CLOCK->EVENTS_LFCLKSTARTED == 0) {}
NRF_RTC0->TASKS_STOP = 0;
```

3.3 [36] CLOCK: Some registers are not reset when expected

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

After watchdog timeout reset, CPU lockup reset, soft reset, or pin reset, the following CLOCK peripheral registers are not reset:

- CLOCK->EVENTS_DONE
- CLOCK->EVENTS_CTTO
- CLOCK->CTIV

Conditions

After watchdog timeout reset, CPU Lockup reset, soft reset, and pin reset.

Consequences

Register reset values might be incorrect. It may cause undesired interrupts in case of enabling interrupts without clearing the DONE or CTTO events.

Workaround

Clear affected registers after reset. This workaround has already been added into system_nrf52.c file. This workaround has already been added into system_nrf52840.c file present in MDK 8.11.0 or later.

3.4 [51] I2S: Aligned stereo slave mode does not work

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

Sample values for the left channel are transmitted twice (for both channels within a frame), sample values for the right channel are lost.

Conditions

CONFIG.MODE = SLAVE, CONFIG.CHANNELS = STEREO, CONFIG.FORMAT = ALIGNED.

Consequences

Aligned format cannot be used for stereo transmission in Slave mode.

Workaround

None.

3.5 [54] I2S: Wrong LRCK polarity in Aligned mode

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

In Aligned mode, left and right samples are swapped.

Conditions

CONFIG.FORMAT = ALIGNED

Consequences

Left and right audio channels are swapped.

Workaround

Swap left and right samples in memory.

3.6 [55] I2S: RXPTRUPD and TXPTRUPD events asserted after STOP

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

The RXPTRUPD event is generated when the STOP task is triggered, even though reception (RX) is disabled. Similarly, the TXPTRUPD event is generated when the STOP task is triggered, even though transmission (TX) is disabled.

Conditions

A previous transfer has been performed with RX/TX enabled, respectively.

Consequences

The indication that RXTXD.MAXCNT words were received/transmitted is false.

Workaround

Ignore the RXPTRUPD and TXPTRUPD events after triggering the STOP task. Clear these events before starting the next transfer.

3.7 [58] SPIM: An additional byte is clocked out when RXD.MAXCNT = 1

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

SPIM clocks out additional byte.

Conditions

RXD.MAXCNT = 1

TXD.MAXCNT <= 1

Consequences

Additional byte is redundant.

Workaround

Use the SPI module (deprecated but still available) or use the following workaround with SPIM:

```
/**
 * @brief Work-around for transmitting 1 byte with SPIM.
 *
 * @param spim: The SPIM instance that is in use.
 * @param ppi_channel: An unused PPI channel that will be used by the
 workaround.
 * @param gpiote_channel: An unused GPIOTE channel that will be used by
 the workaround.
 *
 * @warning Must not be used when transmitting multiple bytes.
 * @warning After this workaround is used, the user must reset the PPI
 channel and the GPIOTE channel before attempting to transmit multiple
 bytes.
 */
void setup_workaround_for_ftpan_58(NRF_SPIM_Type * spim, uint32_t
 ppi_channel, uint32_t gpiote_channel)
{
    // Create an event when SCK toggles.
    NRF_GPIOTE->CONFIG[gpiote_channel] = (
        GPIOTE_CONFIG_MODE_Event <<
        GPIOTE_CONFIG_MODE_Pos
        ) | (
        spim->PSEL.SCK <<
        GPIOTE_CONFIG_PSEL_Pos
        ) | (
        GPIOTE_CONFIG_POLARITY_Toggle <<
        GPIOTE_CONFIG_POLARITY_Pos
        );

    // Stop the spim instance when SCK toggles.
    NRF_PPI->CH[ppi_channel].EEP = (uint32_t)&NRF_GPIOTE-
>EVENTS_IN[gpiote_channel];
    NRF_PPI->CH[ppi_channel].TEP = (uint32_t)&spim->TASKS_STOP;
```

```
    NRF_PPI->CHENSET = 1U << ppi_channel;

    // The spim instance cannot be stopped mid-byte, so it will finish
    // transmitting the first byte and then stop. Effectively ensuring
    // that only 1 byte is transmitted.
}
```

3.8 [66] TEMP: Linearity specification not met with default settings

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

TEMP module provides non-linear temperature readings over the specified temperature range.

Conditions

Always

Consequences

TEMP module returns out of spec temperature readings.

Workaround

Execute the following code after reset:

```
        NRF_TEMP->A0 = NRF_FICR->TEMP.A0;
        NRF_TEMP->A1 = NRF_FICR->TEMP.A1;
        NRF_TEMP->A2 = NRF_FICR->TEMP.A2;
        NRF_TEMP->A3 = NRF_FICR->TEMP.A3;
        NRF_TEMP->A4 = NRF_FICR->TEMP.A4;
        NRF_TEMP->A5 = NRF_FICR->TEMP.A5;
        NRF_TEMP->B0 = NRF_FICR->TEMP.B0;
        NRF_TEMP->B1 = NRF_FICR->TEMP.B1;
        NRF_TEMP->B2 = NRF_FICR->TEMP.B2;
        NRF_TEMP->B3 = NRF_FICR->TEMP.B3;
        NRF_TEMP->B4 = NRF_FICR->TEMP.B4;
        NRF_TEMP->B5 = NRF_FICR->TEMP.B5;
        NRF_TEMP->T0 = NRF_FICR->TEMP.T0;
        NRF_TEMP->T1 = NRF_FICR->TEMP.T1;
        NRF_TEMP->T2 = NRF_FICR->TEMP.T2;
        NRF_TEMP->T3 = NRF_FICR->TEMP.T3;
        NRF_TEMP->T4 = NRF_FICR->TEMP.T4;
```

This code is already present in the latest system_nrf52.c file.

3.9 [68] CLOCK: EVENTS_HFCLKSTARTED can be generated before HFCLK is stable

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

EVENTS_HFCLKSTARTED may come before HFXO is started.

Conditions

When using a 32 MHz crystal with start-up longer than 400 µs.

Consequences

Performance of radio and peripheral requiring HFXO will be degraded until the crystal is stable.

Workaround

32 MHz crystal oscillator startup time must be verified by the user. If the worst-case startup time is shorter than 400 µs, no workaround is required. If the startup time can be longer than 400 µs, the software must ensure, using a timer, that the crystal has had enough time to start up before using peripherals that require the HFXO. The Radio requires the HFXO to be stable before use. The ADC, TIMERs, and TEMP sensor for example can use the HFXO as a reference for improved accuracy.

3.10 [81] GPIO: PIN_CNF is not retained when in debug interface mode

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

GPIO pin configuration is reset on wakeup from System OFF.

Conditions

The system is in debug interface mode.

Consequences

GPIO state unreliable until PIN_CNF is reconfigured.

3.11 [83] TWIS: STOPPED event occurs twice if the STOP task is triggered during a transaction

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

STOPPED event is set after clearing it.

Conditions

The STOP task is triggered during a transaction.

Consequences

STOPPED event occurs twice: When the STOP task is fired and when the master issues a stop condition on the bus. This could provoke an extra interrupt or a failure in the TWIS driver.

Workaround

The last STOPPED event must be accounted for in software.

3.12 [87] CPU: Unexpected wake from System ON Idle when using FPU

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

The CPU is unexpectedly awoken from System ON Idle.

Conditions

The FPU has been used.

Consequences

The CPU is awoken from System ON Idle.

Workaround

The FPU can generate pending interrupts just like other peripherals, but unlike other peripherals there are no INTENSET, INTENCLR registers for enabling or disabling interrupts at the peripheral level. In order to prevent unexpected wake-up from System ON Idle, add this code before entering sleep:

```
#if (__FPU_USED == 1)
 _set_FPSCR(_get_FPSCR() & ~(0x0000009F));
 (void) __get_FPSCR();
 NVIC_ClearPendingIRQ(FPU_IRQn);
#endif
 __WFE();
```

3.13 [89] TWI: Static 400 µA current while using GPIOTE

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

Static current consumption between 400 µA to 450 µA when using TWI in combination with GPIOTE.

Conditions

- GPIOTE is configured in event mode
- TWI utilizes EasyDMA

Consequences

Current consumption higher than specified

Workaround

Turn the TWI off and back on after it has been disabled. To do so: If TWI0 is used,

```
*(volatile uint32_t *)0x40003FFC = 0;
*(volatile uint32_t *)0x40003FFC;
*(volatile uint32_t *)0x40003FFC = 1;
```

If TWI1 is used,

```
*(volatile uint32_t *)0x40004FFC = 0;
*(volatile uint32_t *)0x40004FFC;
*(volatile uint32_t *)0x40004FFC = 1;
```

write 0 followed by a 1 to the POWER register (address 0xFFC) of the TWI that needs to be disabled. Reconfiguration of TWI is required before next usage.

3.14 [94] USBD: BUSSTATE register is not functional

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

BUSSTATE register is not functional.

Conditions

Always.

Consequences

Reading BUSSTATE will not show the state of the bus as documented. No impact on USB 2.0 compliance.

Workaround

None.

3.15 [96] I2S: DMA buffers can only be located in the first 64 kB of data RAM

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

The I2S will not read and write the RAM location specified by the data pointer.

Conditions

DMA buffers are located entirely or in part above address 0x2000 FFFF.

Consequences

Data or memory corruption

Workaround

Set DMA buffers to use memory range 0x2000 0000 to 0x2000 FFFF.

3.16 [98] NFCT: Not able to communicate with the peer

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

The NFCT is not able to receive or transmit messages to the peer.

Conditions

Always

Consequences

The NFCT cannot communicate with the peer.

Workaround

Write 0x00038148 to 0x4000568C before the NFC peripheral is enabled:

```
*(volatile uint32_t *)0x4000568Cul = 0x00038148ul;
```

The workaround is included in the system_nrf52840.c file present in MDK 8.11.0 or later.

3.17 [101] CLOCK: Sleep current increases after soft reset

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

Sleep current with LFXO active is 0.5 µA higher than expected.

Conditions

Low frequency crystal oscillator is active, due to use of RTC or WDT, and a soft-reset is issued or a CPU lock-up reset occurs.

Consequences

Increased sleep current.

Workaround

None.

3.18 [103] CCM: Reset value of CCM.MAXPACKETSIZE causes encryption, decryption, and MIC failures

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

Failing encryption, decryption, and MIC on extended length packets.

Conditions

Always for extended length packets.

Consequences

Failing encryption, decryption, and MIC on extended length packets.

Workaround

Set CCM.MAXPACKETSIZE to 0xFB.

This workaround has already been added into the system_nrf52840.c file present in MDK 8.11.1 or later.

3.19 [104] USBD: EPDATA event is not always generated

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

The EPDATA event might not be generated, and the related update of EPDATASTATUS does not occur.

Conditions

Sometimes.

Consequences

It is not possible to develop a custom USB stack.

Workaround

Use the USB stack provided in Nordic's SDK.

3.20 [110] RADIO: Packet loss or degraded sensitivity

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

In BLE Long Range or 802.15.4 modes, subsequent packets after the first packet might not be received. In BLE and proprietary modes, the sensitivity might be degraded.

Conditions

Always.

Consequences

Might lose packets in BLE LR or 802.15.4 mode. Might lose some sensitivity in BLE and proprietary mode.

Workaround

Always disable the radio after having received a packet (using TASK_DISABLE). The workaround is included in the S132 and S140 SoftDevice.

3.21 [111] RAM: Retention in OFF mode is not controlled by RAM[n].POWER->SxRETENTION, but by RAM[n].POWER->SxPOWER

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

Current consumption in OFF mode is higher than expected. RAM contents are retained in OFF mode when they should not be.

Conditions

Always.

Consequences

Cannot independently control RAM retention in OFF mode and power in ON mode.

Workaround

Use RAM[n].POWER->SxPOWER to control the retention in OFF mode and power in ON mode. Exercise caution when using this workaround, becausee the firmware requires a certain amount of RAM to be powered when waking from OFF mode (such as the RAM where the call stack is located), and RAM[n].POWER registers are retained registers.

3.22 [112] RADIO: False SFD field matches in IEEE 802.15.4 mode RX

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

False FRAMESTART, ADDRESS, PAYLOAD, and END events are triggered and a corrupted packet with a failing CRC is received.

Conditions

The SFD octet of the packet on air does not match the value configured in the SFD register.

Consequences

Packet with CRC error is received, when it should have been discarded based on SFD field.

Workaround

Check for CRC failure after the END event triggers.

3.23 [113] COMP: Single-ended mode with external reference is not functional

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

COMP output is not correct,

Conditions

COMP is used in single-ended mode with external reference.

Consequences

COMP cannot be used in this mode.

Workaround

None.

3.24 [115] RAM: RAM content cannot be trusted upon waking up from System ON Idle or System OFF mode

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

RAM not correctly retained.

Conditions

System ON Idle mode or System OFF is used with parts or all RAM retained.

Consequences

RAM not correctly retained.

Workaround

Apply the following code after any reset:

```
(volatile uint32_t *)0x40000EE4 = ( (*(volatile uint32_t *)0x40000EE4 &
 0x00000070) | // Keep bit 6:4
                                    (*(uint32_t *)0x10000258 &
 0x0000000F) ); // Replace bit 3:0
```

This workaround has already been added into system_nrf52840.c file present in MDK 8.11.0 or later. This workaround increases the I_RAM current per 4 KB section from 20 nA to 30 nA.

3.25 [116] NFCT: HFCLK not stopped when entering into SENSE_FIELD state

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

Higher current consumption than specified in SENSE_FIELD state.

Conditions

The NFCT is going from ACTIVATED state to SENSE_FIELD state.

Consequences

Higher current consumption in SENSE_FIELD state.

Workaround

- Do not use the FIELDLOST_SENSE shortcut in NFCT.
- Do not use a PPI channel to short FIELDLOST event and SENSE task in NFCT.
- When the FIELDLOST event is triggered in NFCT, write 0x01 to address 0x40005010. Then trigger the SENSE task in NFCT to go into SENSE_FIELD state.

3.26 [117] System: Reading address 0x40029618 blocks the device

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

The debugger interface is lost. The device halts or seems to stop executing.

Conditions

Reading address 0x40029618ul, either directly from firmware or with the debugger (for example, using a memory window in the IDE).

Consequences

Crash. Need to power cycle the device and restart the debugging session.

Workaround

Do not read address 0x40029618ul.

3.27 [118] QSPI: Reading halfwords or bytes from the XIP region is not supported

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

The CPU is interrupted with a bus fault.

Conditions

The CPU reads a halfword or a byte from the XIP region. The following instructions could cause a byte or halfword load:

- LDRB
- LDRBT
- LDREXB
- LDRSB
- LDRSBT
- LDRH
- LDRHT
- LDREXH
- LDRSH
- LDRSHT
- TBB
- TBH

Consequences

Cannot run code from external memory.

Workaround

Link the firmware such that the run-time location of the read-only data section is in internal flash or RAM. Also, do not write assembly or C code that reads byte or halfword sized data from external flash.

ARM® Compiler armcc	To prevent the generation of TBB and TBH instructions, use the compiler command line option `--execute_only`. This option will also prevent the generation of instructions that read literals from code sections.
GNU ARM Embedded Toolchain	Using version Q3 2016 or later, you can prevent the generation of TBB and TBH instructions by using the compiler option `-mpure-code`. This option will also prevent the generation of instructions that read literals from the .text section.

3.28 [119] POWER: Wake up from System OFF on V_{BUS} detect is not functional

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

In System OFF mode, the device will not wake up when V_{BUS} supply is connected.

Conditions

Always.

Consequences

The device remains is System OFF mode.

Workaround

External circuitry can be used to translate V_{BUS} voltage levels to GPIO voltage levels that can be used to trigger a GPIO DETECT signal (configured using the GPIOTE peripheral) to wake from System OFF.

3.29 [121] QSPI: Second read and long read commands fail

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

- QSPI read command never gets sent.
- QSPI read command of more than 0x20 characters fails.

Conditions

QSPI.IFCONFIG1 is different than 0xYY0404YY, where Y is any value.

Consequences

QSPI is not functional.

Workaround

When writing IFCONFIG1, make sure to write 0x0404 to IFCONFIG1[23:8].

3.30 [122] QSPI: QSPI uses current after being disabled

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

Current consumption is too high.

Conditions

After QSPI has been activated by the use of TASKS_ACTIVATE task.

Consequences

Current consumption is too high.

Workaround

Execute the following code before disabling QSPI:

```
*(volatile uint32_t *)0x40029010ul = 1ul;
```

3.31 [127] UARTE: Two stop bit setting is not functional

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

Setting CONFIG.STOP=Two (2 stop bits) has no effect.

Conditions

Always.

Consequences

UARTE traffic with 2 stop bit setting is not supported.

Workaround

None

3.32 [128] PDM: RATIO register is not functional

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

The RATIO register is not functional.

Conditions

Always.

Consequences

The only supported ratio between PDM_CLK and output audio sample rate is 64.

Workaround

None.

3.33 [129] USBD: Reading EPSTALL register causes undefined behavior

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

Reading the EPSTALL register locks up the APB bus.

Conditions

Always.

Consequences

Software crashes.

Workaround

Do not read the EPSTALL register. Only write it.

3.34 [130] USBD: Writing to certain read-only registers causes undefined behavior

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

Writing to the following read-only registers locks up the APB bus:

- HALTEDEPIN[0:7]
- HALTEDEPOUT[0:7]
- USBADDR
- DMASTATE
- BMREQUESTTYPE
- BREQUEST
- WVALUEL
- WVALUEH
- WINDEXL
- WINDEXH
- WLENGTHL
- WLENGTHH
- EPOUTSIZE[0:7]
- ISOOUTSIZE8

- FRAMECNTR

Conditions

Always.

Consequences

Software crashes.

Workaround

Do not write these registers. Only read them.

3.35 [131] UARTE: EasyDMA transfer size is limited to 255 bytes

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

DMA transfer is not as long as configured. Only the 8 least significant bits of RXD.MAXCNT and TXD.MAXCNT registers are functional.

Conditions

RXD.MAXCNT and/or TXD.MAXCNT are configured for DMA transfers > 255 bytes.

Consequences

EasyDMA transfer sizes longer than 255 bytes are not supported. Larger size values are treated modulo 256.

Workaround

Split long transfers into chunks of 255 bytes or less.

3.36 [133] CLOCK,RADIO: NRF_RADIO->EVENTS_BCMATCH event might trigger twice

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

A task might be triggered twice by the NRF_RADIO->EVENTS_BCMATCH event.

Conditions

- The NRF_RADIO->EVENTS_BCMATCH event is used to trigger tasks through PPI or SHORTS.
- BCC is set to match after one more bit than the packet size during TX.

Consequences

Tasks connected through PPI or SHORTS to this event might be triggered twice.

Workaround

None.

3.37 [134] USBD: ISOINCONFIG register is not functional

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

The ISOINCONFIG register is not functional

Conditions

Always.

Consequences

Not possible to change the behavior of the ISO IN endpoint response to an IN token when no data is to be sent. The USBD will not respond to the IN token in this situation.

Workaround

None.

3.38 [135] USBD: SIZE.ISOOUT register does not report empty incoming packets

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

The SIZE.ISOOUT register does not report empty incoming packets in the ZERO field.

Conditions

Always.

Consequences

The firmware cannot rely on the ZERO field to know if a zero-length ISO OUT packet has been received.

Workaround

None.

3.39 [136] System: Bits in RESETREAS are set when they should not be

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

After pin reset, RESETREAS bits other than RESETPIN might also be set.

Conditions

A pin reset has triggered.

Consequences

If the firmware evaluates RESETREAS, it might take the wrong action.

Workaround

When RESETREAS shows a pin reset (RESETPIN), ignore other reset reason bits.

Important: RESETREAS bits must be cleared between resets.

3.40 [140] POWER: REG0 External circuitry supply in LDO mode is not functional in System ON IDLE

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

External circuitry supply does not work. A BOR might occur.

Conditions

Using REG0 in LDO mode in System ON IDLE.

Consequences

External circuitry supply cannot be used to supply current >1 mA in System ON IDLE.

Workaround

Use REG0 in DCDC mode.

3.41 [142] RADIO: Sensitivity not according to specification

This anomaly applies to IC Rev. Engineering A, build codes QIAA-AA0.

Symptoms

Radio receiver sensitivity is 3 dB lower than specified.

Conditions

All radio modes.

Consequences

Reduction in receiver sensitivity.

Workaround

None.