nRF52832 Rev 1 Errata v1.0

2016-02-17

Contents

Chapter 1
nRF52832 Rev 1 Errata v1.0

This Errata document contains anomalies for the nRF52832 chip, revision Rev 1 (QFAA-B00, CHAA-B00, QFAB-B00).

The document indicates which anomalies are fixed, inherited, or new compared to revision Engineering C.

Chapter 2
Change log

See the following list for an overview of changes from previous versions of this document.

Table 1: Change log

Version	Date	Change
nRF52832 Rev 1 v1.0	17.02.2016	• Added: No. 12. “Reference ladder is not correctly calibrated” • Added: No. 15. “RAM[x].POWERSET/CLR read as zero” • Added: No. 20. “Register values are invalid” • Added: No. 31. “Calibration values are not correctly loaded from FICR at reset” • Added: No. 36. “Some registers are not reset when expected” • Added: No. 51. “Aligned stereo slave mode does not work” • Added: No. 54. “Wrong LRCK polarity in Aligned mode” • Added: No. 55. “RXPTRUPD and TXPTRUPD events asserted after STOP” • Added: No. 58. “An additional byte is clocked out when RXD.MAXCNT = 1” • Added: No. 64. “Only full bytes can be received or transmitted, but supports 4-bit frame transmit” • Added: No. 66. “Linearity specification not met with default settings” • Added: No. 67. “Some events cannot be used with the PPI” • Added: No. 68. “EVENTS_HFCLKSTARTED can be generated before HFCLK is stable” • Added: No. 72. “TASKS_ACTIVATE cannot be used with the PPI” • Added: No. 74. “Started events fires prematurely” • Added: No. 75. “Increased current consumption” • Added: No. 76. “READY event is set sooner than it should” • Added: No. 77. “RC oscillator is not calibrated when first started” • Added: No. 78. “High current consumption when using timer STOP task only” • Added: No. 79. “ A false EVENTS_FIELDDETECTED event occurs after the field is lost” • Added: No. 81. “PIN_CNF is not retained when in debug interface mode” • Added: No. 83. “STOPPED event occurs twice if the STOP task is triggered during a transaction”

Chapter 3
New and inherited anomalies

The following anomalies are present in revision Rev 1 of the nRF52832 chip.

Table 2: New and inherited anomalies

ID	Module	Description	Inherited from Engineering C
12	COMP	Reference ladder is not correctly calibrated	X
15	POWER	RAM[x].POWERSET/CLR read as zero	X
20	RTC	Register values are invalid	X
31	CLOCK	Calibration values are not correctly loaded from FICR at reset	X
36	CLOCK	Some registers are not reset when expected	X
51	I2S	Aligned stereo slave mode does not work	X
54	I2S	Wrong LRCK polarity in Aligned mode	X
55	I2S	RXPTRUPD and TXPTRUPD events asserted after STOP	X
58	SPIM	An additional byte is clocked out when RXD.MAXCNT = 1	X
64	NFCT	Only full bytes can be received or transmitted, but supports 4-bit frame transmit	X
66	TEMP	Linearity specification not met with default settings	X
67	NFCT,PPI	Some events cannot be used with the PPI	X
68	CLOCK	EVENTS_HFCLKSTARTED can be generated before HFCLK is stable	X
72	NFCT,PPI	TASKS_ACTIVATE cannot be used with the PPI	X
74	SAADC	Started events fires prematurely	X
75	MWU	Increased current consumption	X
76	LPCOMP	READY event is set sooner than it should	X
77	CLOCK	RC oscillator is not calibrated when first started	X
78	TIMER	High current consumption when using timer STOP task only	X
79	NFCT	A false EVENTS_FIELDDETECTED event occurs after the field is lost	X
81	GPIO	PIN_CNF is not retained when in debug interface mode	X
83	TWIS	STOPPED event occurs twice if the STOP task is triggered during a transaction	X

3.1 [12] COMP: Reference ladder is not correctly calibrated

This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, CHAA-B00, QFAB-B00.

It was inherited from the previous IC revision Engineering C.

3.1 Symptoms

COMP does not compare correctly.

3.1 Conditions

Always.

3.1 Consequences

COMP module is unusable.

3.1 Workaround

Execute the following code before enabling the COMP module:

```
*(volatile uint32_t *)0x40013540 = (*(volatile uint32_t *)0x10000324 &
 0x00001F00) >> 8;
```

3.2 [15] POWER: RAM[x].POWERSET/CLR read as zero

This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, CHAA-B00, QFAB-B00.

It was inherited from the previous IC revision Engineering C.

3.2 Symptoms

RAM[x].POWERSET and RAM[x].POWERCLR read as zero, even though the RAM is on.

3.2 Conditions

Always

3.2 Consequences

Not possible to read the RAM state using RAM[x].POWERSET and RAM[x].POWERCLR registers. Write works as it should.

3.2 Workaround

Use RAM[x].POWER to read the state of the RAM.

3.3 [20] RTC: Register values are invalid

This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, CHAA-B00, QFAB-B00.

It was inherited from the previous IC revision Engineering C.

3.3 Symptoms

RTC registers will not contain the correct/expected value if read.

3.3 Conditions

The RTC has been idle.

3.3 Consequences

RTC configuration cannot be determined by reading RTC registers.

3.3 Workaround

Execute the below code before you use RTC.

```
NRF_CLOCK->EVENTS_LFCLKSTARTED  = 0;
NRF_CLOCK->TASKS_LFCLKSTART     = 1;
while (NRF_CLOCK->EVENTS_LFCLKSTARTED == 0) {}
NRF_RTC0->TASKS_STOP = 0;
```

3.4 [31] CLOCK: Calibration values are not correctly loaded from FICR at reset

This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, CHAA-B00, QFAB-B00.

It was inherited from the previous IC revision Engineering C.

3.4 Symptoms

RCOSC32KICALLENGTH is initialized with the wrong FICR value.

3.4 Conditions

Always

3.4 Consequences

RCOSC32KICALLENGTH default value is wrong.

3.4 Workaround

Execute the following code after reset:

```
*(volatile uint32_t *)0x4000053C = ((*(volatile uint32_t *)0x10000244) &
0x0000E000) >> 13;
```

This code is already present in the latest system_nrf52.c file.

3.5 [36] CLOCK: Some registers are not reset when expected

This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, CHAA-B00, QFAB-B00.

It was inherited from the previous IC revision Engineering C.

3.5 Symptoms

After watchdog timeout reset, CPU lockup reset, soft reset, or pin reset, the following CLOCK peripheral registers are not reset: CLOCK->EVENTS_DONE, CLOCK->EVENTS_CTTO, CLOCK->CTIV

3.5 Conditions

After watchdog timeout reset, CPU Lockup reset, soft reset, and pin reset.

3.5 Consequences

Register reset values might be incorrect. It may cause undesired interrupts in case of enabling interrupts without clearing the DONE or CTTO events.

3.5 Workaround

Clear affected registers after reset. This workaround has already been added into system_nrf52.c file.

3.6 [51] I2S: Aligned stereo slave mode does not work

This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, CHAA-B00, QFAB-B00.

It was inherited from the previous IC revision Engineering C.

3.6 Symptoms

Sample values for the left channel are transmitted twice (for both channels within a frame), sample values for the right channel are lost.

3.6 Conditions

CONFIG.MODE = SLAVE, CONFIG.CHANNELS = STEREO, CONFIG.FORMAT = ALIGNED.

3.6 Consequences

Aligned format cannot be used for stereo transmission in Slave mode.

3.6 Workaround

None.

3.7 [54] I2S: Wrong LRCK polarity in Aligned mode

This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, CHAA-B00, QFAB-B00.

It was inherited from the previous IC revision Engineering C.

3.7 Symptoms

In Aligned mode, left and right samples are swapped.

3.7 Conditions

CONFIG.FORMAT = ALIGNED

3.7 Consequences

Left and right audio channels are swapped.

3.7 Workaround

Swap left and right samples in memory.

3.8 [55] I2S: RXPTRUPD and TXPTRUPD events asserted after STOP

This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, CHAA-B00, QFAB-B00.

It was inherited from the previous IC revision Engineering C.

3.8 Symptoms

The RXPTRUPD event is generated when the STOP task is triggered, even though reception (RX) is disabled. Similarly, the TXPTRUPD event is generated when the STOP task is triggered, even though transmission (TX) is disabled.

3.8 Conditions

A previous transfer has been performed with RX/TX enabled, respectively.

3.8 Consequences

The indication that RXTXD.MAXCNT words were received/transmitted is false.

3.8 Workaround

Ignore the RXPTRUPD and TXPTRUPD events after triggering the STOP task. Clear these events before starting the next transfer.

3.9 [58] SPIM: An additional byte is clocked out when RXD.MAXCNT = 1

This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, CHAA-B00, QFAB-B00.

It was inherited from the previous IC revision Engineering C.

3.9 Symptoms

SPIM clocks out additional byte.

3.9 Conditions

RXD.MAXCNT = 1

TXD.MAXCNT <= 1

3.9 Consequences

Additional byte is redundant.

3.9 Workaround

Use the SPI module (deprecated but still available) or use the following workaround with SPIM:

```
/**
 * @brief Work-around for transmitting 1 byte with SPIM.
 *
 * @param spim: The SPIM instance that is in use.
```

```
 * @param ppi_channel: An unused PPI channel that will be used by the
 workaround.
 * @param gpiote_channel: An unused GPIOTE channel that will be used by
 the workaround.
 *
 * @warning Must not be used when transmitting multiple bytes.
 * @warning After this workaround is used, the user must reset the PPI
 channel and the GPIOTE channel before attempting to transmit multiple
 bytes.
 */
void setup_workaround_for_ftpan_58(NRF_SPIM_Type * spim, uint32_t
 ppi_channel, uint32_t gpiote_channel)
{
    // Create an event when SCK toggles.
    NRF_GPIOTE->CONFIG[gpiote_channel] = (
        GPIOTE_CONFIG_MODE_Event <<
        GPIOTE_CONFIG_MODE_Pos
        ) | (
        spim->PSEL.SCK <<
        GPIOTE_CONFIG_PSEL_Pos
        ) | (
        GPIOTE_CONFIG_POLARITY_Toggle <<
        GPIOTE_CONFIG_POLARITY_Pos
        );

    // Stop the spim instance when SCK toggles.
    NRF_PPI->CH[ppi_channel].EEP = (uint32_t)&NRF_GPIOTE-
>EVENTS_IN[gpiote_channel];
    NRF_PPI->CH[ppi_channel].TEP = (uint32_t)&spim->TASKS_STOP;
    NRF_PPI->CHENSET = 1U << ppi_channel;

    // The spim instance cannot be stopped mid-byte, so it will finish
    // transmitting the first byte and then stop. Effectively ensuring
    // that only 1 byte is transmitted.
}
```

3.10 [64] NFCT: Only full bytes can be received or transmitted, but supports 4-bit frame transmit

This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, CHAA-B00, QFAB-B00.

It was inherited from the previous IC revision Engineering C.

3.10 Symptoms

Data bits are not transmitted, or appear to not be received, if the Frame length is not a multiple of 8 bits (i.e. Frame includes data bits).

3.10 Conditions

Frame length is not a multiple of 8 bits (bytes only). Exception: 4-bit frame transmit supported.

3.10 Consequences

Partial bytes cannot be transferred:

- TXD.AMOUNT.TXDATABITS must be 0
- RXD.AMOUNT.RXDATABITS must be 0

3.10 Workaround

None

3.11 [66] TEMP: Linearity specification not met with default settings

This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, CHAA-B00, QFAB-B00.

It was inherited from the previous IC revision Engineering C.

3.11 Symptoms

TEMP module provides non-linear temperature readings over the specified temperature range.

3.11 Conditions

Always

3.11 Consequences

TEMP module returns out of spec temperature readings.

3.11 Workaround

Execute the following code after reset:

```
NRF_TEMP->A0 = NRF_FICR->TEMP.A0;
NRF_TEMP->A1 = NRF_FICR->TEMP.A1;
NRF_TEMP->A2 = NRF_FICR->TEMP.A2;
NRF_TEMP->A3 = NRF_FICR->TEMP.A3;
NRF_TEMP->A4 = NRF_FICR->TEMP.A4;
NRF_TEMP->A5 = NRF_FICR->TEMP.A5;
NRF_TEMP->B0 = NRF_FICR->TEMP.B0;
NRF_TEMP->B1 = NRF_FICR->TEMP.B1;
NRF_TEMP->B2 = NRF_FICR->TEMP.B2;
NRF_TEMP->B3 = NRF_FICR->TEMP.B3;
NRF_TEMP->B4 = NRF_FICR->TEMP.B4;
NRF_TEMP->B5 = NRF_FICR->TEMP.B5;
NRF_TEMP->T0 = NRF_FICR->TEMP.T0;
NRF_TEMP->T1 = NRF_FICR->TEMP.T1;
NRF_TEMP->T2 = NRF_FICR->TEMP.T2;
NRF_TEMP->T3 = NRF_FICR->TEMP.T3;
NRF_TEMP->T4 = NRF_FICR->TEMP.T4;
```

This code is already present in the latest system_nrf52.c file.

3.12 [67] NFCT,PPI: Some events cannot be used with the PPI

This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, CHAA-B00, QFAB-B00.

It was inherited from the previous IC revision Engineering C.

3.12 Symptoms

The following NFCT events do not trigger tasks when used with the PPI:

- EVENTS_AUTOCOLRESSTARTED
- EVENTS_COLLISION

- EVENTS_SELECTED
- EVENTS_STARTED

3.12 Conditions

PPI is used to trigger peripheral tasks using the NFCT events.

3.12 Consequences

The PPI cannot be used to trigger tasks using the following NFCT events:

- EVENTS_AUTOCOLRESSTARTED
- EVENTS_COLLISION
- EVENTS_SELECTED
- EVENTS_STARTED

3.12 Workaround

The EVENTS_AUTOCOLRESSTARTED cannot be used with the PPI.

Subtract an offset of 0x04 while configuring the PPI event end points for the following NFCT events:

- EVENTS_COLLISION
- EVENTS_SELECTED
- EVENTS_STARTED

Examples:

```
NRF_PPI->CH[x].EEP = ((uint32_t) &NRF_NFCT->EVENTS_COLLISION) - 0x04;
NRF_PPI->CH[x].EEP = ((uint32_t) &NRF_NFCT->EVENTS_SELECTED) - 0x04;
NRF_PPI->CH[x].EEP = ((uint32_t) &NRF_NFCT->EVENTS_STARTED) - 0x04;
```

3.13 [68] CLOCK: EVENTS_HFCLKSTARTED can be generated before HFCLK is stable

This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, CHAA-B00, QFAB-B00.

It was inherited from the previous IC revision Engineering C.

3.13 Symptoms

EVENTS_HFCLKSTARTED may come before HFXO is started.

3.13 Conditions

When using a 32 MHz crystal with start-up longer than 400 µs.

3.13 Consequences

Performance of radio and peripheral requiring HFXO will be degraded until the crystal is stable.

3.13 Workaround

32 MHz crystal oscillator startup time must be verified by the user. If the worst-case startup time is shorter than 400 µs, no workaround is required. If the startup time can be longer than 400 µs, the software must ensure, using a timer, that the crystal has had enough time to start up before using peripherals that require the HFXO.

The Radio requires the HFXO to be stable before use. The ADC, TIMERs, and TEMP sensor for example can use the HFXO as a reference for improved accuracy.

3.14 [72] NFCT,PPI: TASKS_ACTIVATE cannot be used with the PPI

This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, CHAA-B00, QFAB-B00.

It was inherited from the previous IC revision Engineering C.

3.14 Symptoms

The NFCT peripheral does not get activated when the PPI is configured to trigger TASKS_ACTIVATE on any event.

3.14 Conditions

Always

3.14 Consequences

The TASKS_ACTIVATE cannot be used with the PPI.

3.14 Workaround

None

3.15 [74] SAADC: Started events fires prematurely

This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, CHAA-B00, QFAB-B00.

It was inherited from the previous IC revision Engineering C.

3.15 Symptoms

False EVENTS_STARTED

3.15 Conditions

TACQ <= 5 µs

3.15 Consequences

The EVENTS_STARTED can come when not expected

3.15 Workaround

The module must be fully configured before it is enabled, and the TACQ configuration must be the last configuration set before ENABLE.

3.16 [75] MWU: Increased current consumption

This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, CHAA-B00, QFAB-B00.

It was inherited from the previous IC revision Engineering C.

3.16 Symptoms

Increased current consumption in System ON IDLE.

3.16 Conditions

When MWU is enabled.

3.16 Consequences

Increased current consumption in System ON IDLE.

3.16 Workaround

Do not use MWU or disable MWU before WFE/WFI, enable it on IRQ.

3.17 [76] LPCOMP: READY event is set sooner than it should

This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, CHAA-B00, QFAB-B00.

It was inherited from the previous IC revision Engineering C.

3.17 Symptoms

May receive unexpected events and wakeups from LPCOMP.

3.17 Conditions

LPCOMP is configured to send an event or to wake up the chip. LPCOMP.TASKS_START task is set and LPCOMP.EVENTS_READY event has been received.

3.17 Consequences

Unpredictable system behavior caused by falsely triggered events and wakeups.

3.17 Workaround

Use the following configuration sequence.

1. Configure the LPCOMP to send an event or wake up the chip, but do not enable any PPI channels or IRQ to be triggered from the LPCOMP events.
2. Trigger the LPCOMP.TASKS_START task and wait for the LPCOMP.EVENTS_READY event.
3. After receiving the LPCOMP.EVENTS_READY event wait for 115 µs.
4. After 115 µs, clear the LPCOMP.EVENTS_DOWN, LPCOMP.EVENTS_UP, and LPCOMP.EVENTS_CROSS events. LPCOMP is now ready to be used.

3.18 [77] CLOCK: RC oscillator is not calibrated when first started

This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, CHAA-B00, QFAB-B00.

It was inherited from the previous IC revision Engineering C.

3.18 Symptoms

The LFCLK RC oscillator frequency can have a frequency error of up to -25 to +40% after reset. A +/- 2% error is stated in the Product Specification.

3.18 Conditions

Always

3.18 Consequences

The LFCLK RC oscillator frequency is inaccurate.

3.18 Workaround

Calibrate the LFCLK RC oscillator before its first use after a reset.

3.19 [78] TIMER: High current consumption when using timer STOP task only

This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, CHAA-B00, QFAB-B00.

It was inherited from the previous IC revision Engineering C.

3.19 Symptoms

Increased current consumption when the timer has been running and the STOP task is used to stop it.

3.19 Conditions

The timer has been running (after triggering a START task) and then it is stopped using a STOP task only.

3.19 Consequences

Increased current consumption

3.19 Workaround

Use the SHUTDOWN task after the STOP task or instead of the STOP task.

3.20 [79] NFCT: A false EVENTS_FIELDDETECTED event occurs after the field is lost

This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, CHAA-B00, QFAB-B00.

It was inherited from the previous IC revision Engineering C.

3.20 Symptoms

A false EVENTS_FIELDDETECTED event occurs.

3.20 Conditions

The task TASK_SENSE is triggered within 150 µs of the event EVENTS_FIELDLOST.

3.20 Consequences

EVENTS_FIELDDETECTED will occur after a field is lost. (SHORT between eventfieldlost and taskSense should not be used since a false fieldDetected event will occur from using the task.)

3.20 Workaround

Wait 150 µs after an EVENTS_FIELDLOST event before triggering TASK_SENSE.

3.21 [81] GPIO: PIN_CNF is not retained when in debug interface mode

This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, CHAA-B00, QFAB-B00.

It was inherited from the previous IC revision Engineering C.

3.21 Symptoms

GPIO pin configuration is reset on wakeup from System OFF.

3.21 Conditions

The system is in debug interface mode.

3.21 Consequences

GPIO state unreliable until PIN_CNF is reconfigured..

3.22 [83] TWIS: STOPPED event occurs twice if the STOP task is triggered during a transaction

This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, CHAA-B00, QFAB-B00.

It was inherited from the previous IC revision Engineering C.

3.22 Symptoms

STOPPED event is set after clearing it.

3.22 Conditions

The STOP task is triggered during a transaction.

3.22 Consequences

STOPPED event occurs twice: When the STOP task is fired and when the master issues a stop condition on the bus. This could provoke an extra interrupt or a failure in the TWIS driver.

3.22 Workaround

The last STOPPED event must be accounted for in software.